Apple //e Soft Switch, Status, and other I/O Locations

December 6,2019

New Memory Management Soft Switches

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| **Address** | **Access** | **Name** | **Description** | **Notes** |
| 0xC000 | W | STR80OFF | Disable 80 column store | 1 |
| 0xC001 | W | STR80ON | Enable 80 column store | 1 |
| 0xC002 | W | RAMRDOFF | Read enable Main RAM, 0x0200-0xBFFF | 2 |
| 0xC003 | W | RAMRDON | Read enable AUX RAM, 0x0200-0xBFFF | 2 |
| 0xC004 | W | RAMWROFF | Write enable Main RAM, 0x0200-0xBFFF | 2 |
| 0xC005 | W | RAMWRON | Write enable AUX RAM, 0x0200-0xBFFF | 2 |
| 0xC006 | W | CXROMOFF | Enable slot ROMs, slots 1-7, or 0xC100-0xC7FF | 3 |
| 0xC007 | W | CXROMON | Enable internal CX00 ROM, or 0xC100-0xCFFF | 3 |
| 0xC008 | W | AUXZPOFF | Enable Main ZP, stack, language card, Av1 BSR RAM | 4 |
| 0xC009 | W | AUXZPON | Enable AUX ZP, stack, language card, AV1 BSR RAM | 4 |
| 0xC00A | W | C3ROMOFF | Enable internal CX3 ROM, 0xC300-0xC3FF |  |
| 0xC00B | W | C3ROMON | Enable Slot ROM, 0xC300-0xC3FF |  |

New Video Soft Switches

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| **Address** | **Access** | **Name** | **Description** | **Notes** |
| 0xC00C | W | VID80OFF | Disable 80 column video |  |
| 0xC00D | W | VID80ON | Enable 80 column video |  |
| 0xC00E | W | ALTCHOFF | Enable normal Apple ][ character set |  |
| 0xC00F | W | ALTCHON | Enable normal alternate character set (no flash) |  |

New Soft Switch Status Flags

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| **Address** | **Access** | **Name** | **Description** | **Clear** | **Set** | **Notes** |
| 0xC000 | R7 | KEY | Read keyboard input | No key | Yes key |  |
| 0xC010 | R7 | CLRKEY | Clear keyboard strobe | No key | Yes key |  |
| 0xC011 | R7 | RDBANK2 | Which LC BANK in use | BANK1 | BANK2 |  |
| 0xC012 | R7 | RDLCRAM | LC RAM or ROM read enabled | ROM | LC RAM |  |
| 0xC013 | R7 | RDRAMRD | Main or AUX RAM read enabled | AUX | Main |  |
| 0xC014 | R7 | RDRAMWR | Main or AUX RAM writ enabled | AUX | Main |  |
| 0xC015 | R7 | RDCXROM | Slot or internal ROM enabled | Slot | Internal |  |
| 0xC016 | R7 | RDAUXZP | Which ZP & LC enabled | Main | AUX |  |
| 0xC017 | R7 | RDC3ROM | Slot or CX ROM enabled | Slot ROM | CX3 ROM |  |
| 0xC018 | R7 | RDSTR80 | State of STR80 switch | Disabled | Enabled |  |
| 0xC019 | R7 | RDVRTBLK | State of vertical blanking | Yes | No |  |
| 0xC01A | R7 | RDTEXT | State of TEXT switch | Graphics | Text |  |
| 0xC01B | R7 | RDMIXED | Read MIXED switch | Off | On |  |
| 0xC01C | R7 | RDPAGE2 | State of PAGE2 switch | PAGE1/Main | PAGE2/AUX |  |
| 0xC01D | R7 | RDHIRES | State of Graphics resolution | LOWRES | HIRES |  |
| 0xC01E | R7 | RDALTCH | State of Alternate Char. Set | Off | On |  |
| 0xC01F | R7 | RDVID80 | State of VID80 video | Disabled | Enabled |  |
| 0xC07E | R7 | RDIOUDIS | Read IOUDIS switch | DHIRES On | DHIRES Off | 5 |
| 0xC07F | R7 | RDDHIRES | Read DHIRES switch | Off | On | 5 |

Cassette, Speaker, Strobes, Video Soft Switches, Annunciators, Controllers

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| **Address** | **Access** | **Name** | **Description** | **Notes** |
| 0xC020 | R | TAPEOUT | Cassette output Toggle |  |
| 0xC030 | R | SPKRTOGL | Speaker output Toggle |  |
| 0xC040 | R | UTILTOGL | Utility Strobe; 1 ms pulse on Game I/O pin 5 |  |
| 0xC050 | R/W | TEXTOFF | Display Graphics |  |
| 0xC051 | R/W | TEXTON | Display Text |  |
| 0xC052 | R/W | MIXEDOFF | Full Screen graphics | 6 |
| 0xC053 | R/W | MIXEDON | Text with graphics | 6 |
| 0xC054 | R/W | PAGE1ON | Display Page 1 or Main video memory | 7 |
| 0xC055 | R/W | PAGE2ON | Display Page 2 or Aux video memory | 7 |
| 0xC056 | R/W | HIRESOFF | Select low resolution Graphics | 6 |
| 0xC057 | R/W | HIRESON | Select high resolution Graphics | 6 |
| 0xC058 | R/W | ANN1OFF | Annunciator 1 off (active if IOUDIS off) |  |
| 0xC059 | R/W | ANN1ON | Annunciator 1 on (active if IOUDIS off) |  |
| 0xC05A | R/W | ANN2OFF | Annunciator 2 off (active if IOUDIS off) |  |
| 0xC05B | R/W | ANN2ON | Annunciator 2 on (active if IOUDIS off) |  |
| 0xC05C | R/W | ANN3OFF | Annunciator 3 off (active if IOUDIS off) |  |
| 0xC05D | R/W | ANN3ON | Annunciator 3 on (active if IOUDIS off) |  |
| 0xC05E | R/W | ANN4OFF | Annunciator 4 off (active if IOUDIS off) |  |
| 0xC05E | R/W | DHRESON | Double HIRES on (active if IOUDIS on) |  |
| 0xC05F | R/W | ANN4ON | Annunciator 4 on (active if IOUDIS off) |  |
| 0xC05F | R/W | DHRESOFF | Double HIRES off (active if IOUDIS on) |  |
| 0xC060 | R | TAPEIN | Cassette input | 8 |
| 0xC061 | R | PB1IN | Push Button 1 input | 8 |
| 0xC062 | R | PB2IN | Push Button 2 input | 8 |
| 0xC063 | R | PB3IN | Push Button 3 input | 8 |
| 0xC064 | R | GC1IN | Game Controller 1 input | 9 |
| 0xC065 | R | GC2IN | Game Controller 2 input | 9 |
| 0xC066 | R | GC3IN | Game Controller 3 input | 9 |
| 0xC067 | R | GC4IN | Game Controller 4 input | 9 |
| 0xC070 | R | GCTOGL | Game Controller Strobe; resets game controllers |  |
| 0xC073 | W | BANKSEL | RamWorks Bank Select; 64 KB bank select |  |
| 0xC07E | W | IODISON | Disable annunciators, enable double HIRES |  |
| 0xC07F | W | IODISOFF | Enable annunciators, disable double HIRES |  |

Original Memory Management Soft Switches for 0xD000-0xDFFF

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| --- | --- | --- | --- | --- |
| **Address** | **Access** | **Name** | **Description** | **Notes** |
| 0xC080 | R | RAM2WP | Select Bank 2; write protect RAM |  |
| 0xC081 | R | RR | ROM2WE | Deselect Bank 2; enable ROM | write enable RAM |  |
| 0xC082 | R | ROM2WP | Deselect Bank 2; enable ROM; write protect RAM |  |
| 0xC083 | R | RR | RAM2WE | Select Bank 2 | write enable RAM |  |
| 0xC084 |  |  | See 0xC080 |  |
| 0xC085 |  |  | See 0xC081 |  |
| 0xC086 |  |  | See 0xC082 |  |
| 0xC087 |  |  | See 0xC083 |  |
| 0xC088 | R | RAM1WP | Select Bank 1; write protect RAM |  |
| 0xC089 | R | RR | ROM1WE | Deselect Bank 1; enable ROM | write enable RAM |  |
| 0xC08A | R | ROM1WP | Deselect Bank 1; enable ROM; write protect RAM |  |
| 0xC08B | R | RR | RAM1WE | Select Bank 1 | write enable RAM |  |
| 0xC08C |  |  | See 0xC088 |  |
| 0xC08D |  |  | See 0xC089 |  |
| 0xC08E |  |  | See 0xC08A |  |
| 0xC08F |  |  | See 0xC08B |  |

Control Switches for Disk ][

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| --- | --- | --- | --- | --- |
| **Address** | **Access** | **Name** | **Description** | **Notes** |
| 0xC080 | R | PHAS0OFF | Turns stepper motor phase 1 off |  |
| 0xC081 | R | PHAS0ON | Turns stepper motor phase 1 on |  |
| 0xC082 | R | PHAS1OFF | Turns stepper motor phase 2 off |  |
| 0xC083 | R | PHAS1ON | Turns stepper motor phase 2 on |  |
| 0xC084 | R | PHAS2OFF | Turns stepper motor phase 3 off |  |
| 0xC085 | R | PHAS2ON | Turns stepper motor phase 3 on |  |
| 0xC086 | R | PHAS3OFF | Turns stepper motor phase 4 off |  |
| 0xC087 | R | PHAS3ON | Turns stepper motor phase 4 on |  |
| 0xC088 | R | MOTOROFF | Turns motor off |  |
| 0xC089 | R | MOTORON | Turns motor on |  |
| 0xC08A | R | DRV0EN | Selects Drive 1 |  |
| 0xC08B | R | DRV1EN | Selects Drive 2 |  |
| 0xC08C | R | STROBE | Strobe data latch for I/O |  |
| 0xC08D | R/W | LATCH | Load data latch |  |
| 0xC08E | R | DATAIN | Prepare latch for input | 10 |
| 0xC08F | W | DATAOUT | Prepare latch for output | 11 |

1. If STR80OFF access PAGE1/PAGE2 and use RAMRD and RAMWR; if STR80ON access Main or AUX display page (0x400) using PAGE2.
2. If 80STORE is ON these switches do not affect video memory.
3. If INTCXROM in ON then switch SLOTC3ROM is available, otherwise MAIN ROM is accessed.
4. Use Bank enable and write protect switches to control 0xD000-0xFFFF.
5. Triggers paddle timer and resets VBLINT.
6. This mode is only effective when TEXT switch is OFF.
7. This switch changes function when 80STORE is ON.
8. Data on MSB only.
9. Read 0xC070 first, then count until MSB is zero.
10. DATAIN with STROBE for Read and DATAIN with LATCH for Sense Write Protect.
11. DATAOUT with STROBE for Write and DATAOUT with LATCH for Load Write Latch.

Control Switches for ZIP CHIP

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| --- | --- | --- | --- |
| **Address** | **Access** | **Name** | **Description** |
| 0xC05A | W | ZIPCTRL | 4 writes of 0x5A unlocks ZIP CHIP; 0xA5 locks ZIP CHIP |
| 0xC05B | W | ZIPSTATS | Any byte written enables ZIP CHIP |
| 0xC05B | R | ZIPSTATS | Bits 0 and 1 is RAM size: 0 – 8K, 1 – 16K, 2 – 32K, 3 – 64K; bit 3 for memory delay: 0 – fast mode (no delay), 1 – sync mode (delay); bit 4 is ZIP enable: 0 – enabled, 1 – disabled; bit 5 is paddle speed: 0 - fast, 1 – normal; bit 6 is cache update: 0 – no, 1 - yes; bit 7 is clock pulse every 1.0035 milliseconds |
| 0xC05C | R/W | ZIPSLOTS | Set/read speaker/slot 0 – fast, 1 – normal. Bit 0 - speaker, bits 1 to 7 for slots 1 to 7 |
| 0xC05D | W | ZIPSPEED | Set speed: bit 2 – clk2/3, bit 3 – clk3/4, bit 4 - clk4/5, bit 5 – clk5/6, bit 6 – clk/2, bit 7 – clk/4 |
| 0xC05E | W | ZIPDELAY | Bit 7: 0 – enable delay, 1 – disable and reset delay |
| 0xC05E | R | ZIPDELAY | 0 – off, 1 – on: bit 0 – ROMRD, bit 1 – RAMBNK, bit 2 – RAGE2, bit 3 – HIRES, bit 4 – 80STORE, bit 5 – MWR, bit 6 – MRD, bit 7 - ALTZP |
| 0xC05F | W | ZIPCACHE | Bit 6 paddle delay: 0 – disable, 1 – enable; bit 7 language card cache: 0 – enable, 1 - disable |

Control Switches for CFFA

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| **Address** | **Access** | **Name** | **Description** |
| 0xC080 | R/W | ATADATAH | Read or write high data byte register |
| 0xC081 | R | SETCSMSK | Disable pre-fetch register |
| 0xC082 | R | CLRCSMSK | Enable pre-fetch register |
| 0xC086 | R | ATASTAT2 | Read aternate status register |
| 0xC086 | W | ATADEVCT | Write device control register |
| 0xC088 | R/W | ATADATAL | Read or write low data byte register |
| 0xC089 | R | ATAERROR | Read error register |
| 0xC08A | W | ATASECCT | Write sector count register |
| 0xC08B | W | ATASECTR | Write LBA3 (07:00) address register |
| 0xC08C | W | ATACYLNL | Write LBA2 (15:08) address register |
| 0xC08D | W | ATACYLNH | Write LBA1 (23:16) address register |
| 0xC08E | W | ATAHEAD | Write drive/head configuration register |
| 0xC08F | R | ATASTAT | Read primary status register |
| 0xC08F | W | ATACMD | Write command register |

Control Switches for quikLoader

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| **Address** | **Access** | **Name** | **Description** |
| 0xC080 | W | QLSELC0 | Select banks 0 or 1, on/off, USR, EPROM number |
| 0xC081 | W | QLSELC1 | Select banks 2 or 3, on/off, USR, EPROM number |
| 0xC082 | W | QLSELC2 | Select banks 4 or 5, on/off, USR, EPROM number |
| 0xC083 | W | QLSELC3 | Select banks 6 or 7, on/off, USR, EPROM number |

Control Switches for Sider, RamDisk, RamCard, and RANA

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| **Address** | **Access** | **Name** | **Description** |
| 0xC080 | R | SDINPUT | Read status |
| 0xC080 | W | SDINPUT | Write drive number, DCB data, input data |
| 0xC081 | R | SDOUTPUT | Read output data |
| 0xC081 | W | SDOUTPUT | Write start, flush, and stop commands |
|  |  |  |  |
| 0xC080 | W | RDSECTR | RamDisk sector number |
| 0xC081 | W | RDTRACK | RamDisk track number |
|  |  |  |  |
| 0xC084 | W | RAMCARD | RamCard on/off, track\*2, sector/8 |
|  |  |  |  |
| 0xC800 | W | ROMCODE1 | Select RANA top record head |
| 0xC801 | W | ROMCODE2 | Select RANA bottom record head |